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3.3 V Slew Rate Limited, Half Duplex RS-485/RS-422 Transceiver

ADM3493

FEATURES

Operates with 3.3 V supply
Interoperable with 5 V logic
EIA RS-422 and RS-485 compliant over full CM range
Data rate: 250 kbps
Half duplex transceiver
Reduced slew rates for low EMI
2 nA supply current in shutdown mode
Up to 256 transceivers on a bus
–7 V to +12 V bus common-mode range
Specified over –40°C to +85°C temperature range
8 ns skew
Available in 8-lead SOIC

APPLICATIONS

Low power RS-485 applications
EMI sensitive systems
DTE-DCE interfaces
Industrial control
Packet switching
Local area networks
Level translators

FUNCTIONAL BLOCK DIAGRAM

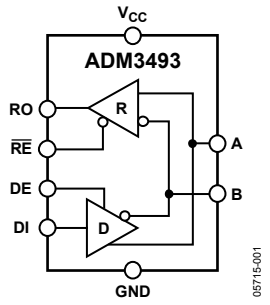

Figure 1.

GENERAL DESCRIPTION

The ADM3493 is a low power, differential line transceiver designed to operate using a single 3.3 V power supply. Low power consumption, coupled with a shutdown mode, makes it ideal for power-sensitive applications. The ADM3493 is suitable for communication on multipoint bus transmission lines.

The device contains one driver and one receiver. Designed for half-duplex communication, the ADM3493 features a slew rate limited driver that minimizes EMI and reduces reflections caused by improperly terminated cables, allowing error-free data transmission at data rates up to 250 kbps.

The receiver input impedance is 96 kΩ, allowing up to 256 transceivers to be connected on the bus. A thermal shutdown circuit prevents excessive power dissipation caused by bus contention or by output shorting. If a significant temperature increase is detected in the internal driver circuitry during fault conditions then the thermal shutdown circuit forces the driver output into a high impedance state. The receiver contains a fail-safe feature that results in a logic high output state, if the inputs are unconnected (floating).

The ADM3493 is fully specified over the commercial and industrial temperature ranges and is available in an 8-lead SOIC.

Rev. 0
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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113 **©2005 Analog Devices, Inc. All rights reserved.**

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REVISION HISTORY

10/05—Rev. 0: Initial Version

SPECIFICATIONS

V_{CC} = 3.3 V ±0.3 V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
DRIVER					
Differential Output Voltage, V_{OD}	2.0			V	R_L = 100 Ω (RS-422), V_{cc} = 3.3 V ±5% (see Figure 3)
	1.5			V	R_L = 54 Ω (RS-485) (see Figure 3)
	1.5			V	R_L = 60 Ω (RS-485), V_{cc} = 3.3 V (see Figure 4)
Δ $\|V_{OD}\|$ for Complementary Output States[1]			0.2	V	R_L = 54 Ω or 100 Ω (see Figure 3)
Common-Mode Output Voltage, V_{OC}			3	V	R_L = 54 Ω or 100 Ω (see Figure 3)
Δ $\|V_{OC}\|$ for Common-Mode Output Voltage[1]			0.2	V	R_L = 54 Ω or 100 Ω (see Figure 3)
DRIVER INPUT LOGIC					
CMOS Input Logic Threshold Low, V_{IH}			0.8	V	DE, DI, $\overline{RE}$
CMOS Input Logic Threshold High, V_{IL}	2.0			V	DE, DI, $\overline{RE}$
CMOS Logic Input Current, I_{N1}			±2	μA	DE, DI, $\overline{RE}$
Input Current (A, B), I_{N2}		60		μA	V_{IN} = 12 V; DE = 0 V
		−60		μA	V_{IN} = −7 V; DE = 0 V, V_{CC} = 0 V or 3.6 V
RECEIVER					
Differential Input Threshold Voltage, V_{TH}	−0.2		0.2	V	−7V < V_{CM} < + 12 V
Input Hysteresis, Δ V_{TH}		50		mV	V_{CM} = 0 V
CMOS Output Voltage High, V_{OH}	V_{cc} − 0.4			V	I_{OUT} = −1.5 mA, V_{ID} = 200 mV (see Figure 5)
CMOS Output Voltage Low, V_{OL}			0.4	V	I_{OUT} = 2.5mA, V_{ID} = 200mV (see Figure 5)
Three-State Output Leakage Current, I_{OZR}			±1	μA	V_{cc} = 3.6 V, 0 V ≤ V_{OUT} ≤ V_{cc}
Input Resistance, R_{IN}		96		kΩ	−7 V < V_{CM} < + 12 V
POWER SUPPLY CURRENT					
Supply Current		1.1	2.2	mA	DE = V_{CC}; $\overline{RE}$ = 0 V or V_{CC}; No load, DI = 0 V or V_{CC}
		0.95	1.9	mA	DE = V_{CC}; $\overline{RE}$ = 0 V; No load, DI = 0 V or V_{CC}
Supply Current in Shutdown Mode, I_{SHDN}		0.002	1	μA	DE = 0 V, $\overline{RE}$ = V_{CC}, DI = V_{CC} or 0 V
Driver Short-Circuit Output Current, I_{OSD}			−250	mA	V_{OUT} = −7 V
			250	mA	V_{OUT} = 12 V
Receiver Short-Circuit Output Current, I_{OSR}	±8		±60	mA	0 V < V_{RO} < V_{CC}

[1] ΔV_{OD} and ΔV_{OC} are the changes in V_{OD} and V_{OC}, respectively, when DI input changes state.

TIMING SPECIFICATIONS

V_{CC} = 3.3 V, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
DRIVER					
Differential Output Delay, t_{DD}	600	900	1400	ns	R_L = 60 Ω (see Figure 6 and Figure 12)
Differential Output Transition Time, t_{TD}	400	700	1200	ns	R_L = 60 Ω (see Figure 6 and Figure 12)
Propagation Delay, Low-to-High Level, t_{PLH}	700	1000	1500	ns	R_L = 27 Ω (see Figure 7 and Figure 13)
Propagation Delay, High-to-Low Level, t_{PHL}	700	1000	1500	ns	R_L = 27 Ω (see Figure 7 and Figure 13)
$\lvert t_{PLH} - t_{PHL} \rvert$ Propagation Delay Skew[1], t_{PDS}		100		ns	R_L = 27 Ω (see Figure 7 and Figure 13)
DRIVER OUTPUT ENABLE/DISABLE TIMES					
Output Enable Time to Low Level, t_{PZL}		900	1300	ns	R_L = 110 Ω (see Figure 9 and Figure 15)
Output Enable Time to High Level, t_{PZH}		600	800	ns	R_L = 110 Ω (see Figure 8 and Figure 14)
Output Disable Time from High Level, t_{PHZ}		50	80	ns	R_L = 110 Ω (see Figure 8 and Figure 14)
Output Disable Time from Low Level, t_{PLZ}		50	80	ns	R_L = 110 Ω (see Figure 9 and Figure 15)
Output Enable Time from Shutdown to Low Level, t_{PSL}		1.9	2.7	µs	R_L = 110 Ω (see Figure 9 and Figure 15)
Output Enable Time from Shutdown to High Level, t_{PSH}		2.2	3.0	µs	R_L = 110 Ω (see Figure 8 and Figure 14)
RECEIVER					
Time to Shutdown[2], t_{SHDN}	80	190	300	ns	
Propagation Delay, Low-to-High Level, t_{RPLH}	25	75	180	ns	V_{ID} = 0 V to 3.0 V, C_L = 15 pF (see Figure 10 and Figure 16)
Propagation Delay, High-to-Low Level, t_{RPHL}	25	75	180	ns	V_{ID} = 0 V to 3.0 V, C_L = 15 pF (see Figure 10 and Figure 16)
$\lvert t_{PLH} - t_{PHL} \rvert$ Propagation Delay Skew, t_{RPDS}			50	ns	V_{ID} = 0 V to 3.0 V, C_L = 15 pF (see Figure 10 and Figure 16)
RECEIVER OUTPUT ENABLE/DISABLE TIMES					
Output Enable Time to Low Level, t_{PRZL}		25	50	ns	C_L = 15 pF (see Figure 11 and Figure 17)
Output Enable Time to High Level, t_{PRZH}		25	50	ns	C_L = 15 pF (see Figure 11 and Figure 17)
Output Disable Time from High Level, t_{PRHZ}		25	45	ns	C_L = 15 pF (see Figure 11 and Figure 17)
Output Disable Time from Low Level, t_{PRLZ}		25	45	ns	C_L = 15 pF (see Figure 11 and Figure 17)
Output Enable Time from Shutdown to Low Level, t_{PRSL}		720	1400	ns	C_L = 15 pF (see Figure 11 and Figure 17)
Output Enable Time from Shutdown to High Level, t_{PRSH}		720	1400	ns	C_L = 15 pF (see Figure 11 and Figure 17)

[1] Measured on $\lvert t_{PLH}(A) - t_{PHL}(A) \rvert$ and $\lvert t_{PLH}(B) - t_{PHL}(B) \rvert$.

[2] The transceivers are put into shutdown by bringing $\overline{RE}$ high and DE low. If the inputs are in this state for less than 80 ns, the parts are guaranteed not to enter shutdown. If the inputs are in this state for at least 300 ns, the parts are guaranteed to enter shutdown.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{CC} to GND	7 V
Digital I/O Voltage (DE, $\overline{RE}$, DI)	−0.3 V to V_{CC} + 0.3 V
Digital I/O Voltage (R_{OUT})	V_{CC} − 0.5 V to V_{CC} + 0.5 V
Driver Output/Receiver Input Voltage	−7.5 V to +12.5 V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +125°C
θ_{JA} Thermal Impedance	
8-Lead SOIC	121°C/W
Lead Temperature	
Soldering (10 seconds)	300°C
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

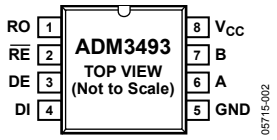


Figure 2. Pin Configuration

Table 4. . Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RO	Receiver Output. When enabled, if A > B by 200 mV, then RO = high. If A < B by 200 mV, then RO = low.
2	$\overline{RE}$	Receiver Output Enable. A low level enables the receiver output, RO. A high level places it in a high impedance state. If $\overline{RE}$ is high and DE is low, the device enters a low power shutdown mode.
3	DE	Driver Output Enable. A high level enables the driver differential Outputs A and B. A low level places it in a high impedance state. If $\overline{RE}$ is high and DE is low, the device enters a low power shutdown mode.
4	DI	Driver Input. When the driver is enabled, a logic low on DI forces A low and B high while a logic high on DI forces A high and B low.
5	GND	Ground.
6	A	Noninverting Receiver Input A and Noninverting Driver Output A.
7	B	Inverted Receiver Input B and Inverted Driver Output B.
8	V_{CC}	Power Supply, 3.3 V ± 0.3 V.

TEST CIRCUITS

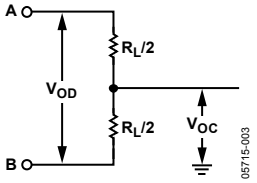


Figure 3. Driver V_{OD} and V_{OC}

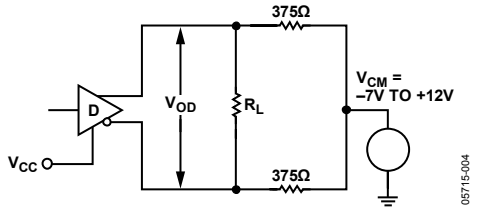


Figure 4. Driver V_{OD} with Varying Common-Mode Voltage

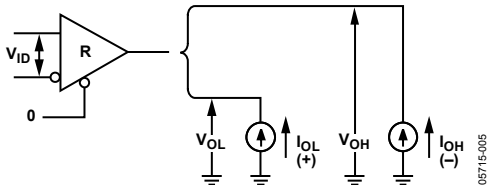
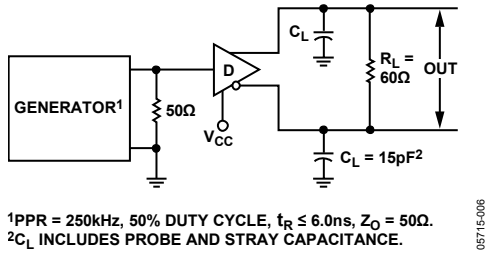
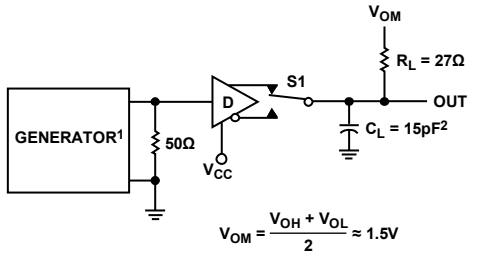


Figure 5. Receiver V_{OH} and V_{OL}



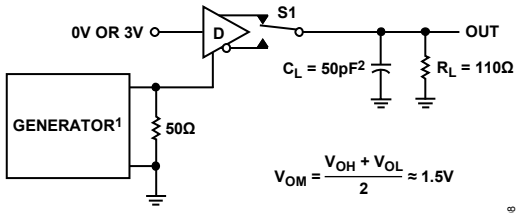
[1]PPR = 250kHz, 50% DUTY CYCLE, $t_R \le 6.0$ns, $Z_O = 50\Omega$.
[2]C_L INCLUDES PROBE AND STRAY CAPACITANCE.

Figure 6. Driver Differential Output Delay and Transition Times



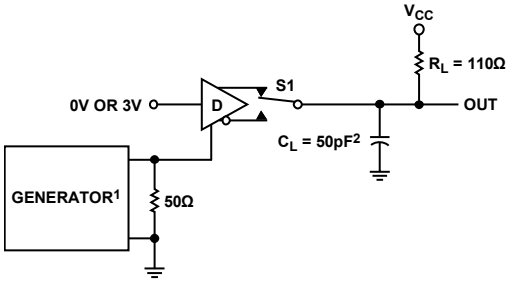
[1]PPR = 250kHz, 50% DUTY CYCLE, $t_R \le 6.0$ns, $Z_O = 50\Omega$.
[2]C_L INCLUDES PROBE AND STRAY CAPACITANCE.

Figure 7. Driver Propagation Delays



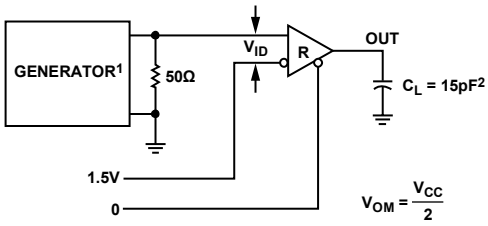
[1]PPR = 250kHz, 50% DUTY CYCLE, $t_R \le 6.0$ns, $Z_O = 50\Omega$.
[2]C_L INCLUDES PROBE AND STRAY CAPACITANCE.

Figure 8. Driver Enable and Disable Times (t_{PZH}, t_{PSH}, t_{PHZ})



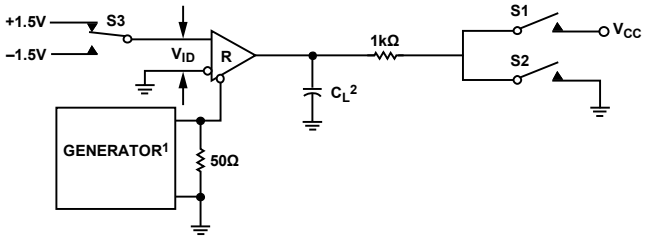
[1]PPR = 250kHz, 50% DUTY CYCLE, $t_R \le 6.0$ns, $Z_O = 50\Omega$.
[2]C_L INCLUDES PROBE AND STRAY CAPACITANCE.

Figure 9. Driver Enable and Disable Times (t_{PZL}, t_{PSL}, t_{PLZ})



[1]PPR = 250kHz, 50% DUTY CYCLE, $t_R \le 6.0$ns, $Z_O = 50\Omega$.
[2]C_L INCLUDES PROBE AND STRAY CAPACITANCE.

Figure 10. Receiver Propagation Delay



[1]PPR = 250kHz, 50% DUTY CYCLE, $t_R \le 6.0$ns, $Z_O = 50\Omega$.
[2]C_L INCLUDES PROBE AND STRAY CAPACITANCE.

Figure 11. Receiver Enable and Disable Times

SWITCHING CHARACTERISTICS

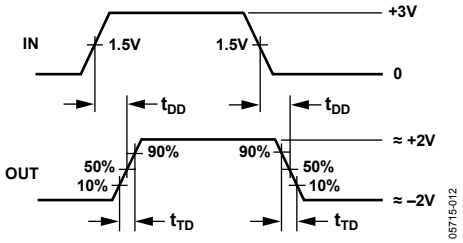


Figure 12. Driver Differential Output Delay and Transition Times

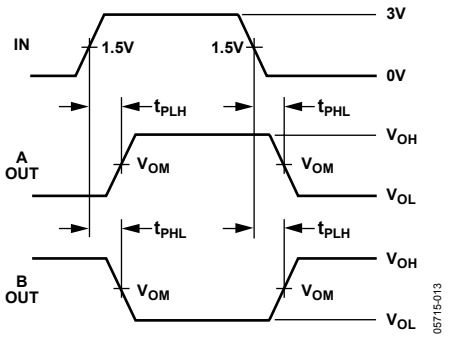


Figure 13. Driver Propagation Delays

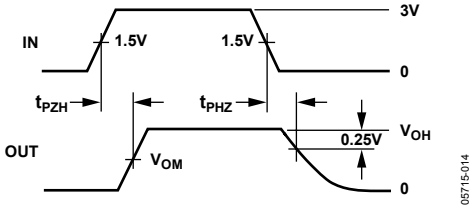


Figure 14. Driver Enable and Disable Times (t_{PZH}, t_{PSH}, t_{PHZ})

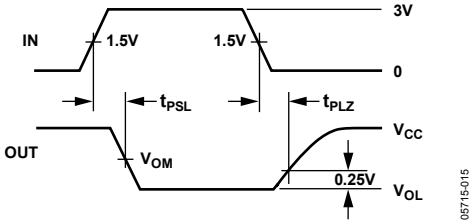


Figure 15. Driver Enable and Disable Times (t_{PZL}, t_{PSL}, t_{PLZ})

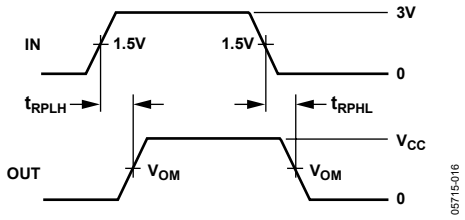


Figure 16. Receiver Propagation Delay

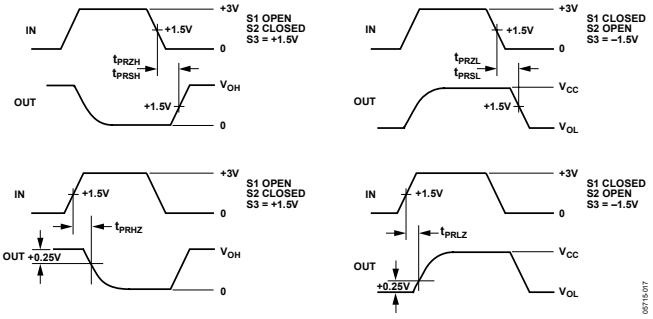


Figure 17. Receiver Enable and Disable Times

TYPICAL PERFORMANCE CHARACTERISTICS

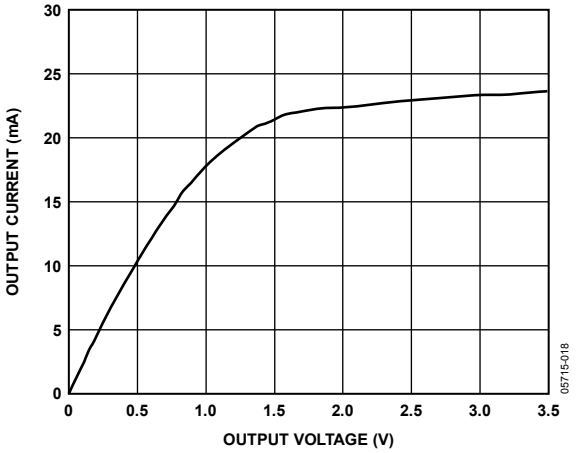


Figure 18. Output Current vs. Receiver Output Low Voltage

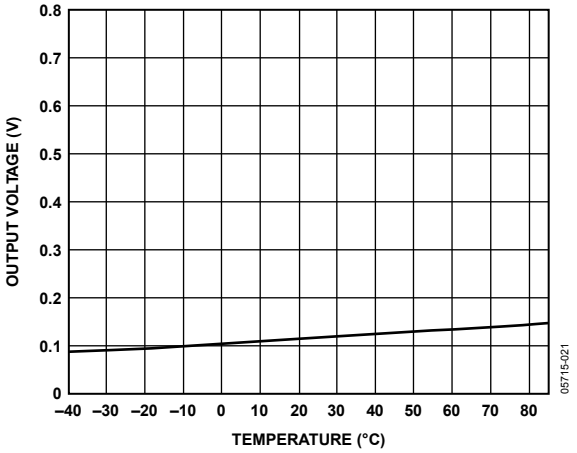


Figure 21. Receiver Output Low Voltage vs. Temperature, I_O = 2.5 mA

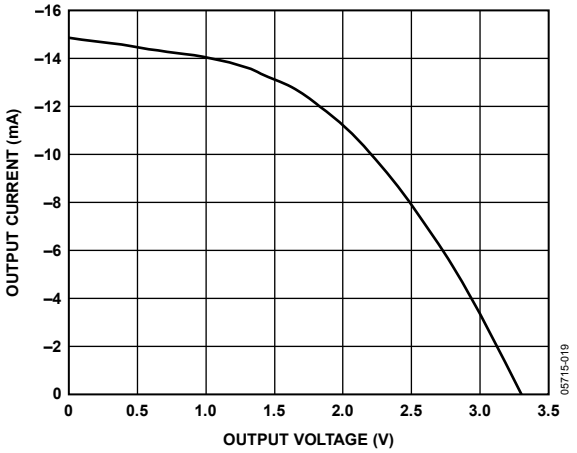


Figure 19. Output Current vs. Receiver Output High Voltage

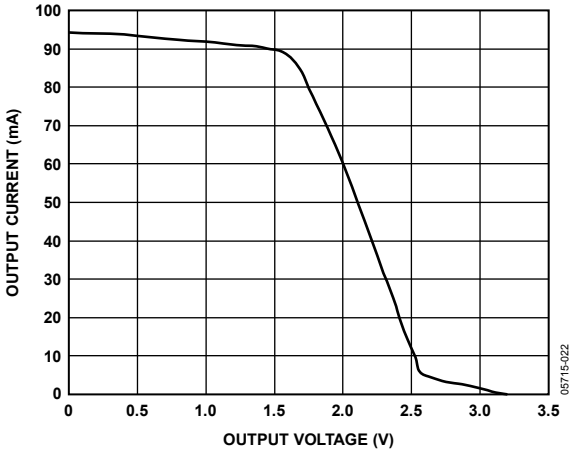


Figure 22. Driver Output Current vs. Differential Output Voltage

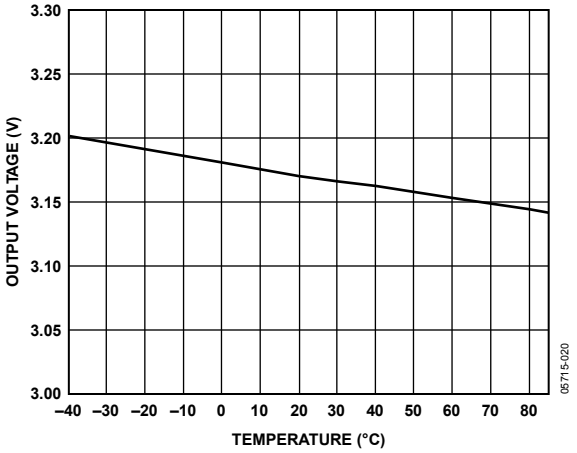


Figure 20. Receiver Output High Voltage vs. Temperature, I_O = 1.5 mA

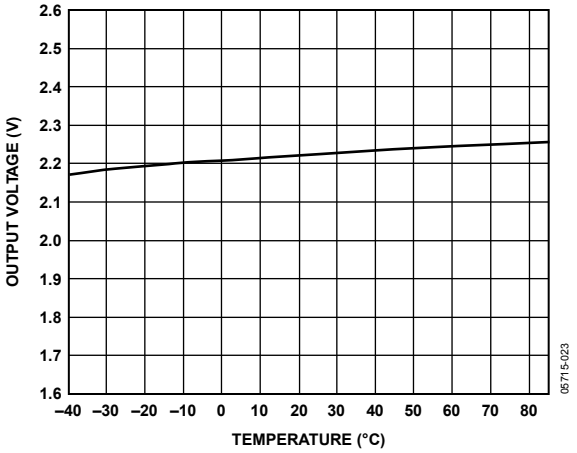


Figure 23. Driver Differential Output Voltage vs. Temperature, RI = 54 Ω

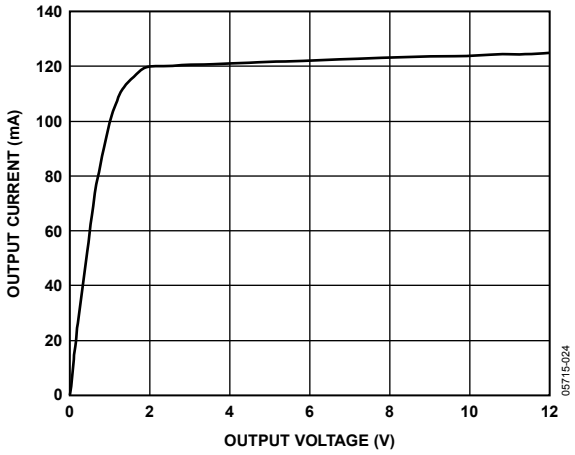


Figure 24. Output Current vs. Driver Output Low Voltage

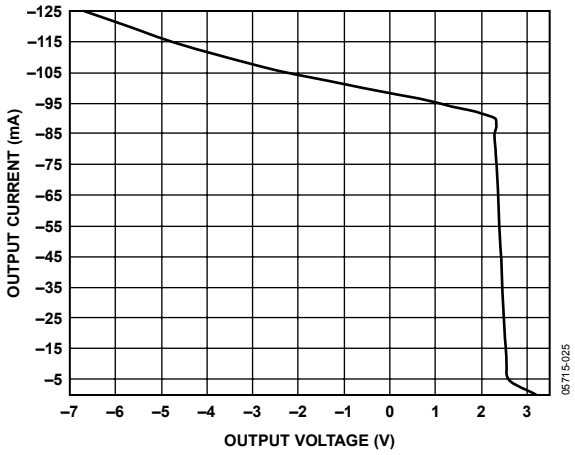


Figure 25. Output Current vs. Driver Output High Voltage

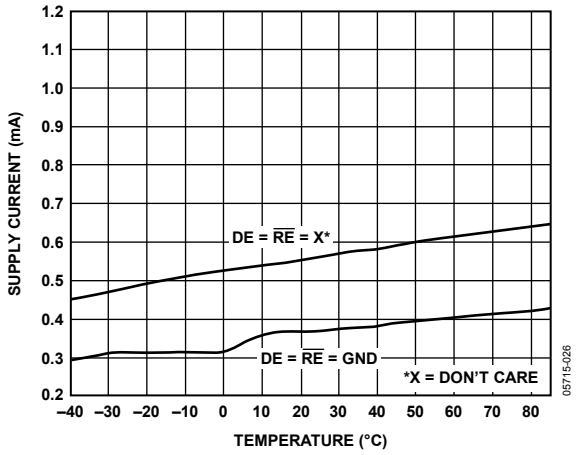


Figure 26. Supply Current vs. Temperature

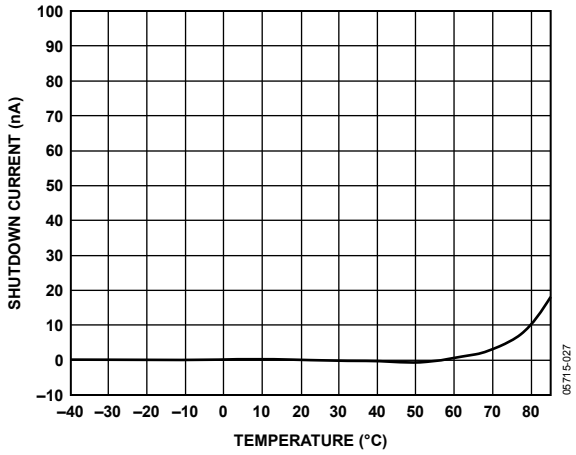


Figure 27. Shutdown Current vs. Temperature, V_{CC} = 3.3 V

CIRCUIT DESCRIPTION

The ADM3493 is a low power transceiver for RS-485 and RS-422 communications. The ADM3493 can transmit and receive at data rates up to 250 kbps in a half duplex configuration. Driver Enable (DE) and Receiver Enable ($\overline{RE}$) pins are included when disabled; the driver and receiver outputs are high impedance.

Table 5. Transmitting Truth Table

Transmitting Inputs			Transmitting Outputs		Mode
$\overline{RE}$	DE	DI	B	A	
X[1]	1	1	0	1	Normal
X[1]	1	0	1	0	Normal
0	0	X[1]	High-Z[2]	High-Z[2]	Normal
1	0	X[1]	High-Z[2]	High-Z[2]	Shutdown

[1] X = Don't care.
[2] High-Z = High Impedance.

Table 6. Receiving Truth Table

Receiving Inputs			Receiving Outputs	Mode
$\overline{RE}$	DE	A - B	RO	
0	0	≥+0.2 V	1	Normal
0	0	≤−0.2 V	0	Normal
0	0	Inputs Open	1	Normal
1	0	X[1]	High-Z[2]	Shutdown

[1] X = Don't care.
[2] High-Z = High Impedance

REDUCED EMI AND REFLECTIONS

The ADM3493 is a slew rate limited transceiver, minimizing EMI and reducing reflections caused by improperly terminated cables.

LOW POWER SHUTDOWN MODE

A low power shutdown mode is initiated by bringing both $\overline{RE}$ high and DE low. The ADM3493 does not shut down unless both the driver and receiver are disabled (high impedance). In shutdown, the ADM3493 typically draws only 2 nA of supply current. For the ADM3493, the t_{PSH} and t_{PSL} enable times assume the part was in the low power shutdown mode; the t_{PZH} and t_{PZL} enable times assume the receiver or driver was disabled, but the part was not shut down.

DRIVER OUTPUT PROTECTION

Two methods are implemented to prevent excessive output current and power dissipation caused by faults or by bus contention. Current limit protection on the output stage provides immediate protection against short circuits over the whole common-mode voltage range (see Typical Performance Characteristics). In addition, a thermal shutdown circuit forces the driver outputs into a high impedance state if the die temperature rises excessively.

PROPAGATION DELAY

Skew time is simply the difference between the low-to-high and high-to-low propagation delay. Small driver/receiver skew times help maintain a symmetrical mark-space ratio (50% duty cycle). The receiver skew time, $|t_{PRLH} - t_{PRHL}|$, is 20 ns for the ADM3493. The driver skew time is typically under 100 ns.

TYPICAL APPLICATIONS

The ADM3493 transceiver is designed for bidirectional data communications on multipoint bus transmission lines. Figure 22 shows a typical network application's circuits. To minimize reflections, the line should be terminated at both ends in its characteristic impedance, and stub lengths off the main line should be kept as short as possible. The slew rate limited ADM3493 is tolerant of imperfect termination.

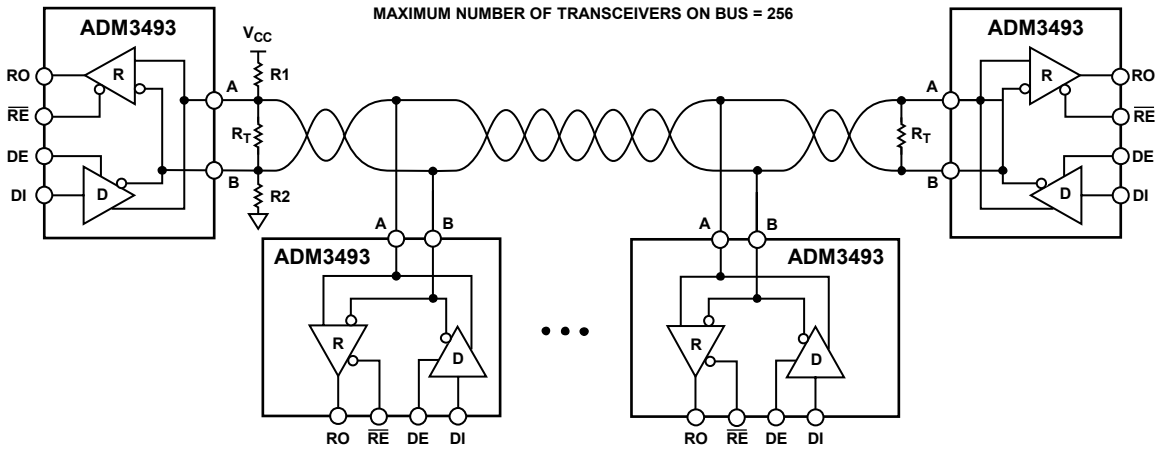
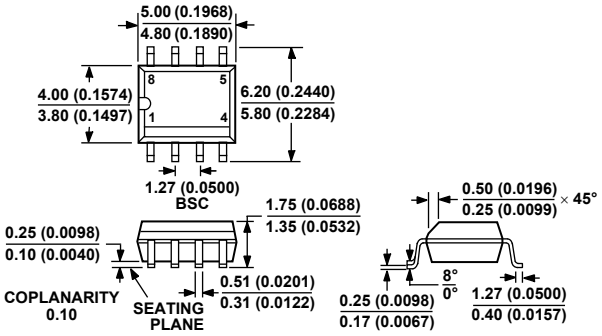


Figure 28. ADM3493 Typical Half Duplex RS-485 Network

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 29. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Options	Ordering Quantity
ADM3493ARZ[1]	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADM3493ARZ-REEL7[1]	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	1,000

[1] Z = Pb-free part.

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